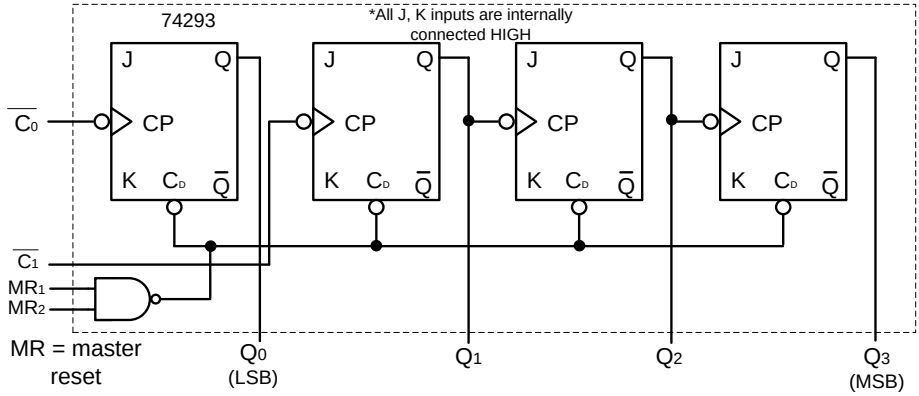
Extra Practice Questions (Part 2)

These questions are provided for your own practice / study. They will not be covered in tutorial classes.

1. The figure below shows the circuitry within the 74'293 counter IC.

(You are only able to access the signals, $\overline{C_0}, \overline{C_1}, MR_1, MR_2, Q_0, Q_1, Q_2, Q_3$, outside of the dotted box.)

Show how you would make use of use one 74'293 IC, one J-K flip-flop and other logic gates to realize an **asynchronous** Mod-29 ripple counter.



2. A synchronous counter counts in the following order : 1, 2, 5, 7, 1 ...

(i) Implement this counter using J-K flip-flops.

(ii) Based on your implementation in (i), describe what happens to your counter if it lands in an invalid state of 3 (eg. counter output is 3)?

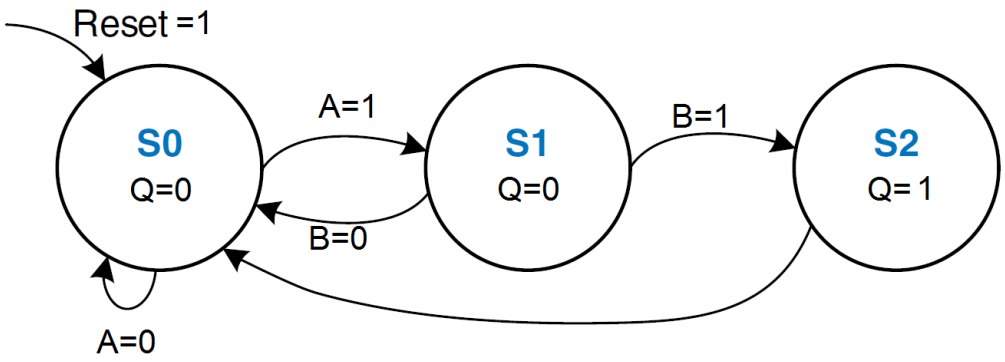
3. The next state table of a FSM with an input A and output Z is given below :

Current State	Next State		Output	
	A = 0	A = 1	A = 0	A = 1
S0	S3	S1	0	0
S1	S2	S0	0	1
S2	S0	S3	1	0
S3	S0	S2	1	1

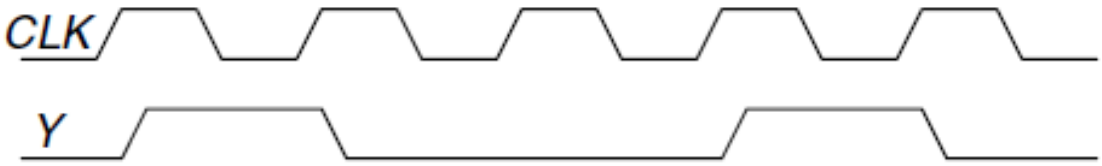
Draw the state transition diagram of this FSM.

Suppose that your current state is unknown. If A is consecutively '0' for two clock cycles, what are the possible state(s) you will be in after two clock cycles?

4. Describe in words what the state machine below does and implement the state machine using D flip-flops with synchronous resets.



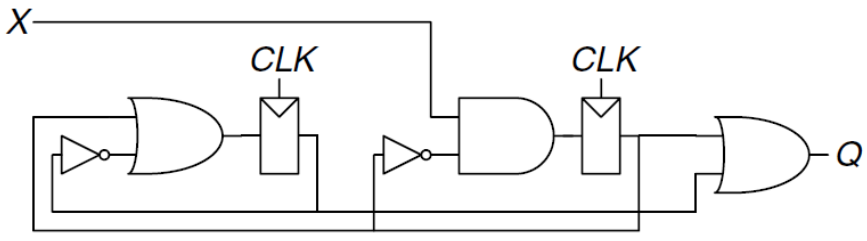
5. A divide-by-N pulse generator has one output and no inputs. The output Y is HIGH for one clock cycle out of every N clock cycles. For N=3, the waveform for a divide-by-3 pulse generator is as shown below.

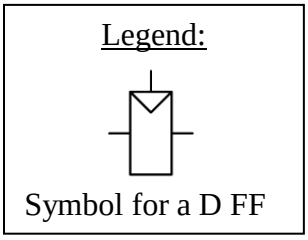


(i) Develop the state transition diagram for the divide-by-3 pulse generator, assuming that the FSM starts at an initial reset state.
(ii) Implement the circuit using only D-FFs and **no additional gates**. You may assume that the D-FFs have synchronous resets or sets.

(Hint : Use one-hot state encoding for the state assignments eg. 3'b001, 3'b010, 3'b100.)

6. Analyze the FSM shown below. Write the state transition table, output logic table and sketch the state transition diagram. Describe whether this is a Mealy or Moore machine and what the FSM does.





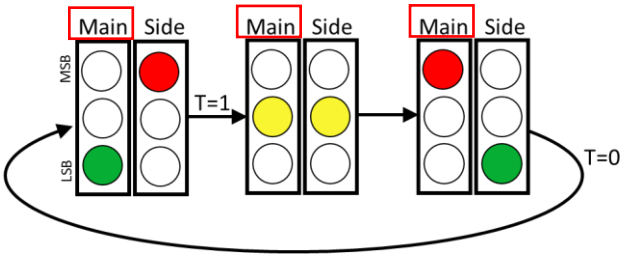
7. A 3-bit synchronous counter counts in one of two sequences depending on a 1-bit synchronous control input, EVEN. When EVEN is false, the counter behaves as a normal 3-bit mod-8 up-counter, otherwise it counts in the sequence: .. 0, 2, 4, 6, 0, 2 …

When the value of EVEN is toggled, it proceeds to the other counting sequence.

(a) Draw the state transition diagram for the counter.
(b) If the counter's current output is "2", under what conditions will it output "3" in the next state?
(c) Implement the counter using D-Flip-flops and any additional logic devices. Clearly show the steps in your design.
(d) Using additional logic gates, show how you would incorporate a "terminal count" output, TC, which is TRUE if the state is 7 and EVEN=0, or if the state is 6 and EVEN=1.

8. You need to design a simple control circuit for the traffic signal at the intersection of a busy main street and a deserted road. A traffic sensor asserts a 1-bit signal **T** when traffic is detected on the side road. Two sets of traffic lights (main and side) need to be controlled as shown in the diagram below. Each traffic light produces a 3-bit output with the MSB and LSB controlling the RED and GREEN respectively.

Design a **counter** using D FFs to control the Main traffic light.



9. Gray codes have a useful property in that consecutive numbers differ in only a single bit position. The table below lists a 3-bit Gray code representing the numbers 0 to 7. Design a 3-bit mod-8 Gray code counter with no inputs and three outputs. When reset, the output should be 000. On each clock edge, the output should advance to the next Gray code. After reaching 100, it should repeat with 000.

Number	Gray code		
0	0	0	0
1	0	0	1
2	0	1	1
3	0	1	0
4	1	1	0
5	1	1	1
6	1	0	1
7	1	0	0

10. Design the state transition diagram for an FSM which has a 2-bit input X and an output Y. The output Y becomes 1 when the cumulative sum of the numbers in sequence X (up to and including the current clock cycle) is a multiple of 3. Assume that Y starts with an initial reset value of TRUE or '1'.

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X :   00   →   11   →   01   →   10   →   00   →   01   …
Y :   1    →   1    →   0    →   1    →   1    →   0
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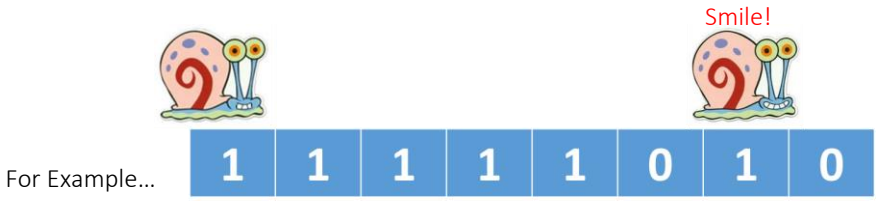
11. Alyssa owns a pet robotic snail with an FSM brain. The snail crawls from left to right along a paper tape containing a sequence of 1's and 0's.



On each clock cycle, the snail crawls to the next bit. The snail smiles when the last four bits that it has crawled over are, from left to right, 1101. The input A is the bit currently underneath the snail's antennae. The output Y is TRUE when the snail smiles. Design a FSM to compute when the snail should smile.

Implement your state transition diagrams for the FSM as a (i) Moore machine (ii) Mealy machine.